

*Contd
B3
C1
C1* forming an upper electrode on the capacitor dielectric layer,
wherein the lower electrode is formed of metal.

2. (Twice amended) The method of claim 1, wherein the lower electrode is formed
of a material selected from the group consisting of ruthenium and platinum.

3. (Cancelled)

*Sub C1
B2* 4. (Once Amended) The method of claim 1, wherein a metal organic material is
used as a source of the CVD method

Sub C1 6. The method of claim 4, wherein the pre-annealing does not substantially change
the materiality of the lower electrode.

*Sub C1
B3* 7. (Twice amended) The method of claim 1, wherein the step of forming a capacitor
dielectric layer comprises:
depositing a capacitor dielectric layer on the pre-annealed lower electrode; and
subjecting the capacitor dielectric layer to a crystallization annealing, wherein a
temperature of the crystallization annealing is lower than an inherent temperature of
crystallization annealing of said capacitor dielectric layer.

8. (Twice amended) The method of claim 6, wherein the pre-annealing is performed
at a range of between 350 ~ 750°C.

9. The method of claim 4, wherein the selected atmosphere comprises a hydrogen
gas.

10. The method of claim 4, wherein the selected atmosphere comprises a nitrogen
gas.

11. The method of claim 4, wherein the selected atmosphere is a mixed atmosphere.

12. ~~The method of claim 11, wherein the mixed atmosphere comprise a hydrogen and a nitrogen gas.~~

Sub-C17
134 13. (Twice amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a lower electrode on a substrate by CVD method using a source having carbon;
subjecting the lower electrode to a pre-annealing for removing carbon remaining in the lower electrode, wherein the pre-annealing is a treatment exposing the lower electrode under a plasma atmosphere;

forming a capacitor dielectric layer on the pre-annealed lower electrode; and

forming an upper electrode on the capacitor dielectric layer,

wherein the lower electrode is formed of metal.

14. (Twice amended) The method of claim 13, wherein the lower electrode is formed of a material selected from the group consisting of ruthenium and platinum.

15. The method of claim 14, wherein a metal organic material is used as a source of the CVD method

17. The method of claim 15, wherein the pre-annealing does not substantially change the materiality of the lower electrode.

Sub-C17
B5 18. (Twice amended) The method of claim 13, wherein the step of forming a capacitor dielectric layer comprises:

depositing a capacitor dielectric layer on the pre-annealed lower electrode; and

subjecting the capacitor dielectric layer to a crystallization annealing, wherein a temperature of the crystallization annealing is lower than an inherent temperature of crystallization annealing of said capacitor dielectric layer.

but 117
19. The method of claim 15, wherein the plasma atmosphere comprises a hydrogen gas.

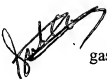
but 117
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20. (Twice amended) A method of fabricating a semiconductor device, comprising the steps of:
forming a lower electrode on a substrate by a CVD method using a source having carbon;
subjecting the lower electrode to a pre-annealing form removing carbon remaining in the lower electrode, wherein the pre-annealing is a treatment exposing the lower electrode under plasma atmosphere;
depositing a tantalum oxide layer on the pre-annealed lower electrode;
crystallizing the tantalum oxide layer; and
forming an upper electrode on the capacitor dielectric layer,
wherein the lower electrode is formed of metal, the pre-annealing is performed at a range of between 350 ~ 750°C, and the materiality and surface form of the lower electrode does not substantially change be the pre-annealing.

21. The method of claim 20, wherein the pre-annealing is one selected from the group consisting of a thermal annealing under a selected atmosphere and a treatment exposing the lower electrode under a plasma atmosphere.

23. (Cancelled)

but 117
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24. (Twice amended) The method of claim 21, wherein a temperature of the crystallization annealing is lower than the inherent temperature of crystallization of said capacitor dielectric layer.

but 117
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25. (Once Amended) The method of claim 24, wherein the inherent crystallizing temperature of the tantalum oxide layer is over 700°C and the crystallizing temperature of the tantalum oxide layer is about 650°C.


 26. The method of claim 21, wherein the selected atmosphere comprises a hydrogen gas and the thermal annealing is performed at about 450°C.

27. The method of claim 21, wherein the selected atmosphere comprises a nitrogen gas and the thermal annealing is performed at about 700°C.

28. The method of claim 21, wherein the selected atmosphere is a mixed atmosphere including about 90% of nitrogen and about 10% of hydrogen by volume.

29. The method of claim 28, wherein the thermal annealing is performed at about 450°C.

30. The method of claim 8, wherein the pre-annealing is performed at about 450°C.

 31. (Once Amended) The method of claim 17, wherein the pre-annealing is performed at a range of between 350 ~ 750°C.

32. The method of claim 31, wherein the pre-annealing is performed at about 450°C.